REMARKS

The Examiner has stated that claim 18 would be allowable. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter.

The Examiner rejected claims 1-17 and 19-30 under 35 U.S.C. §102(b) as being unpatentable over Janesch et al..

Applicants respectfully traverse the §102(b) rejections with the following arguments.

35 USC § 102

The Examiners rejection of claims 1-8 are moot in light of Applicants cancellation of claims 1-8.

The Examiner rejected claim 9 under 35 U.S.C §102(b) stating "Janesch et al discloses a phase adjustable clock circuit comprising: means (220) for generating a first clock signal (I before adjustment) and a second clock signal (Q before adjustment); and means (164) for receiving said first clock signal and for generating a third clock signal (I after adjustment) from said first clock signal and means (164) for receiving said second clock signal and for generating a fourth clock signal (Q after adjustment), wherein at least one of said third and said fourth clock signals differ in phase from said first and said second clock signal respectively."

Applicants contend that claim 9, as amended, is not anticipated by Janesch et al. because Janesch et al. does not teach each and every feature of claim 9.

As a first example Janesch et al. does not teach "a first phase adjustment circuit that receives said first clock signal and that generates a third clock signal from said first clock signal and a second phase adjustment circuit that receives said second clock signal and that generates a fourth clock signal."

First, Applicants point out, Janesch et al. teaches only a single phase detector 164 while Applicants claim requires first and second phase adjustments circuits.

Second, Applicants respectfully point out Janesch et al. phase detector 164 does not generate any clock signals no less two clock signals. Phase detector 164 generates only a single digital phase error signal 165. See Janesch et al. FIG. 2 and col. 6, lines 30-34.

Third, Janesch et al. teaches there are only two clock signals 155a (I) and 155b (Q), not four as the Examiner alleges. Both clock signals 155a (I) and 155b (Q) are generated by voltage

controlled oscillator 220 and supplied back to phase detector 164. See Janesch et al. FIG. 2 and col. 6, line 63 to col. 7 line 1. Further, because of the feedback of clock signals 155a (I) and 155b (Q) in the circuit of Janesch et al. FIG. 2, clock signals 155a (I) and clock signals 155b (Q) are continuously adjusted and because there is no operation performed between voltage controlled oscillator 220 and phase detector 164 there can not be distinct " I before adjustment" and "I after adjustment" signals. Similarly, there can not be distinct " Q before adjustment" and "Q after adjustment" signals. Thus Janesch et al. teaches only first and second clock signals.

As a second example Janesch et al. does not teach "wherein at least one of said third and said fourth clock signals differ in phase from said first and said second clock signal respectively."

Since there are only first and second clock signals (155a and 155b) taught by Janesch et al. it is not possible for "wherein at least one of said third and said fourth clock signals differ in phase from said first and said second clock signal respectively" as Applicants claim 9 requires.

Based on the preceding arguments, Applicants respectfully maintain that claim 9 is not unpatentable over Janesch et al. and is in condition for allowance. Since claims 10-16 and 31-34 depend from claim 9, Applicants respectfully maintain that claims 10-16 and 31-34 are likewise in condition for allowance.

The Examiner rejected claim 17 under 35 U.S.C §102(b) stating "Janesch et al discloses a clock and data recovery circuit comprising: means (220) for generating a first and a second clock signal; means (164) for receiving said first clock signal and for generating a third clock signal from said first clock signal and means (164) for receiving said second clock signal and for generating a fourth clock signal, wherein at least one of said third and said fourth clock signals differ in phase from said first and said second clock signal respectively; means (164) for

receiving said third and fourth clock signals and a serial data stream (Received signal) and for generating a reconstructed serial data stream and a phase error signal; means (166) for receiving said phase error signal and for generating a phase adjustment signal (167) and means (210) for receiving said phase adjustment signal by said clock generation circuit in a feedback loop to adjust the phases of said first and second clock signals."

Applicants contend that claim 17, as amended, is not anticipated by Janesch et al. because Janesch et al. does not teach each and every feature of claim 17.

As a first example Janesch et al. does not teach "a first phase adjustment circuit that receives said first clock signal and that generates a third clock signal from said first clock signal and a second phase adjustment circuit that receives said second clock signal and that generates a fourth clock signal."

First, Applicants point out, Janesch et al. teaches only a single phase detector 164 while Applicants claim requires first and second phase adjustments circuits.

Second, Applicants respectfully point out Janesch et al. phase detector 164 does not generate any clock signals no less two clock signals. Phase detector 164 generates only a single digital phase error signal 165. See Janesch et al. FIG. 2 and col. 6, lines 30-34.

Third, Janesch et al. teaches there are only two clock signals 155a (I) and 155b (Q), not four as the Examiner alleges. Both clock signals 155a (I) and 155b (Q) are generated by voltage controlled oscillator 220 and supplied back to phase detector 164. See Janesch et al. FIG. 2 and col. 6, line 63 to col. 7 line 1. Further, because of the feedback of clock signals 155a (I) and 155b (Q) in the circuit of Janesch et al. FIG. 2, clock signals 155a (I) and clock signals 155b (Q) are continuously adjusted and because there is no operation performed between voltage controlled oscillator 220 and phase detector 164 there can not be distinct " I before adjustment"

and "I after adjustment" signals. Similarly, there can not be distinct " Q before adjustment" and "Q after adjustment" signals. Thus Janesch et al. teaches only first and second clock signals.

As a second example Janesch et al. does not teach "wherein at least one of said third and said fourth clock signals differ in phase from said first and said second clock signal respectively."

Since there are only first and second clock signals (155a and 155b) taught by Janesch et al. it is not possible for "wherein at least one of said third and said fourth clock signals differ in phase from said first and said second clock signal respectively" as Applicants claim 17 requires.

As a third example Janesch et al. does not teach "means for receiving said third and fourth clock signals and a serial data stream and for generating a reconstructed serial data stream and a phase error signal."

Applicants respectfully point out that the Examiner has the phase detector 164 of Janesch et al. receiving the first and second clock signals and both generating and receiving the third and fourth clock signals which is not possible in the circuit of FIG. 2 of Janesch et. al. Further, the Examiner has indicated that loop filter 166 receives a phase error signal [165 from phase detector 164]. Since phase error signal 165 is the only signal being outputted by phase detector 164 it is not possible that the phase detector 164 is also generating the third and fourth clock signals. The only clock generating circuit in Janesch et al. is voltage controlled oscillator 220 and it generates only the first and second clock signals.

Based on the preceding arguments, Applicants respectfully maintain that claim 17 is not unpatentable over Janesch et al. and is in condition for allowance. Since claims 18-30 and 35-38 depend from claim 17, Applicants respectfully maintain that claims 18-30 and 35-38 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR:
Bonanccio et al.

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